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UTILITY PATENT APPLICATION TRANSMITTAL

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Attorney Docket No.	042390.P6892
First Inventor or Application Identifier	Kaizad R. Mistry
Title	FIELD EFFECT TRANSISTOR STRUCTURE WITH SELF-ALIGNED
Express Mail Label No.	EL414968991US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
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1. ☒ Fee Transmittal Form
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2. ☒ Specification [*Total Pages* 25]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (*if filed*)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 10]

4. Oath or Declaration [*Total Pages* 3]
a. ☐ Newly executed (original copy)
b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §§ 1.63(d)(2) and 1.33(b).

5. ☐ Microfiche Computer Program *(Appendix)*

6. Nucleotide and/or Amino Acid Sequence Submission
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7. ☐ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement *(when there is an assignee)* ☐ Power of Attorney
9. ☐ English Translation Document *(if applicable)*
10. ☐ Information Disclosure Statement (IDS)/PTO - 1449 ☐ Copies of IDS Citations
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☐ *Customer Number or Bar Code Label* (Insert Customer No. or Attach bar code label here) *or* ☒ *Correspondence address below*

Name	BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP				
Address	12400 Wilshire Boulevard, Seventh Floor				
City	Los Angeles	*State*	California	*Zip Code*	90025
Country	U.S.A.	*Telephone*	(503) 684-6200	*Fax*	(503) 684-3245

Name (Print/Type)	Gregory D. Caldwell, Reg. No. 39,926		
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P6892 PATENT

FIELD EFFECT TRANSISTOR STRUCTURE WITH SELF-ALIGNED RAISED SOURCE/DRAIN EXTENSIONS

Inventor: Kaizad R. Mistry

"Express Mail" mailing label number EL414960991US

P6892

FIELD EFFECT TRANSISTOR STRUCTURE WITH SELF-ALIGNED RAISED SOURCE/DRAIN EXTENSIONS

Inventor: Kaizad R. Mistry

Background of the Invention

Field of the Invention

The invention relates to metal-oxide-semiconductor field effect transistors (MOSFETs) and more particularly to transistor structures having self-aligned raised source/drain regions, and methods of making same.

Background

The trend of integrating more functions on a single substrate while operating at ever higher frequencies has existed in the semiconductor industry for many years. Advances in both semiconductor process technology and digital system architecture have aided in producing these more highly integrated and faster operating integrated circuits.

The desired result of many recent advances in semiconductor process technology has been to reduce the dimensions of the transistors used to form the individual circuits found on integrated circuits. There are several well-recognized benefits of reducing the size of transistors. In the case of MOSFETs, reducing the channel length provides the capability to deliver a given amount of drive current with a smaller channel width. By reducing the width and length of a FET, the parasitic gate capacitance, which is a function of the area defined by the width and length can be reduced, thereby improving circuit performance. Similarly, reducing the size of transistors is beneficial in that less area is consumed for a given circuit, and this allows more circuits in a given area, or a smaller, less costly chip, or both.

It has also been well known that MOSFETs can not simply be scaled down linearly. That is, as the width and length attributes of a MOSFET are reduced, other parts of the transistor, such as the gate dielectric and the

junctions must also be scaled so as to achieve the desired electrical characteristics. Undesirable electrical characteristics in MOSFETs due to improper scaling include coupling of the electric field into the channel region and increased subthreshold conduction. These effects are sometimes referred to in this field as short channel effects.

A number of methods have been developed to form ever more shallow source/drain junctions for MOSFETs in order to achieve proper scaling. Unfortunately, these very shallow junctions create source/drain extensions that have increased resistivity as compared with deeper source/drain junctions. In longer channel length MOSFETs with deeper source/drain junctions, the source/drain extension resistivity was negligible compared to the on-resistance of the MOSFET itself. However, as MOSFET channel lengths decrease into the deep sub-micron region, the increased source/drain extension resistivity becomes a significant performance limitation.

What is needed is a field effect transistor structure having very short channel length and low source/drain extension resistivity, yet operable to produce high drive currents without suffering from the short channel effects that produce significant levels of off-state current. What is further needed is a method of manufacturing such a structure.

Summary of the Invention

Briefly, field effect transistor structures include a channel regions formed in a recessed portion of a substrate. The recessed channel portion permits the use of relatively thicker source/drain regions thereby providing lower source/drain extension resistivity while maintaining the physical separation needed to overcome various short channel effects.

In a further aspect of the present invention, the surface of the recessed channel portion may be of a rectangular, polygonal, or curvilinear shape.

Brief Description of the Drawings

Fig. 1 is a schematic cross-section of a conventional MOSFET showing symmetrical source/drains with source/drain extensions.

Fig. 2 is a schematic cross-section of a MOSFET having raised source/drain extension in accordance with a first exemplary embodiment of the present invention

Fig. 3 is a schematic cross-section of a MOSFET in accordance with a second exemplary embodiment of the present invention having tapered edges and raised source/drain extensions.

Fig. 4 is a schematic cross-section of a MOSFET in accordance with a third exemplary embodiment of the present invention having a curvilinear gate dielectric and raised source/drain extensions.

Fig. 5 is a schematic cross-section of a wafer having an etch stop layer and an unpatterned damascene layer formed thereon.

Fig. 6 is a schematic cross-section showing the structure of Fig. 5, after the damascene and etch stop layers have been patterned.

Fig. 7 is a schematic cross-section showing the structure of Fig. 6, after a first spacer layer has been formed adjacent to the sidewalls of the patterned damascene and etch stop layers.

Fig. 8 is a schematic cross-section showing the structure of Fig. 7, after the exposed silicon has been anisotropically etched.

Fig. 9 is a schematic cross-section showing the structure of Fig. 8, after the second spacer has been removed, a gate oxide layer grown over the exposed silicon, and a gate electrode layer deposited over the wafer.

Fig. 10 is a schematic cross-section showing the structure of Fig. 9, after the gate electrode is formed by a chemical mechanical polishing operation which removes the excess gate electrode material.

Fig. 11 is a schematic cross-section showing the structure of Fig. 10, after the damascene, first spacer, and etch stop layers have been etched away.

Fig. 12 is a schematic cross-section showing a completed MOSFET formed from the structure of Fig. 11, after conventional processing operations such as source/drain extension implants, gate spacer formation, deep source/drain implants, and silicidation of source/drains and gate electrode.

Fig. 13 is a schematic cross-section showing the structure of Fig. 7, after the exposed silicon has been oxidized, and the exposed oxidized silicon has been etched, forming a recess with tapered.

Fig. 14 is a schematic cross-section showing the structure of Fig. 13, after the second spacer has been removed, a gate oxide layer grown over the exposed silicon, and a gate electrode layer deposited over the wafer.

Fig. 15 is a schematic cross-section showing the structure of Fig. 14, after the gate electrode is formed by a chemical mechanical polishing operation which removes the excess gate electrode material.

Fig. 16 is a schematic cross-section showing the structure of Fig. 15, after the damascene, first spacer, and etch stop layers have been etched away.

Fig. 17 is a schematic cross-section showing a completed MOSFET formed from the structure of Fig. 16, after conventional processing operations such as source/drain extension implants, gate spacer formation, deep source/drain implants, and silicidation of source/drains and gate electrode.

Fig. 18 is a schematic cross-section showing the structure of Fig. 7, after the exposed silicon has been isotropically etched.

Fig. 19 is a schematic cross-section showing the structure of Fig. 18, after the second spacer has been removed, a gate oxide layer grown over the exposed silicon, and a gate electrode layer deposited over the wafer.

Fig. 20 is a schematic cross-section showing the structure of Fig. 19, after the gate electrode is formed by a chemical mechanical polishing operation which removes the excess gate electrode material.

Fig. 21 is a schematic cross-section showing the structure of Fig. 20, after the damascene, first spacer, and etch stop layers have been etched away.

Fig. 22 is a schematic cross-section showing a completed MOSFET formed from the structure of Fig. 21, after conventional processing operations such as source/drain extension implants, gate spacer formation, deep source/drain implants, and silicidation of source/drains and gate electrode.

Fig. 23 is a flow diagram of a process in accordance with the present invention.

Detailed Description

Overview

In order to continue to scale the MOSFET to smaller dimensions, it is necessary to scale both the lateral dimensions (e.g., gate length) as well as the vertical dimensions (e.g., junction depth). In particular, it is required to reduce the depth of the source/drain extension (SDE) as the dimensions of the MOSFET are scaled down, so as to reduce short channel effects. However, as SDE depth is reduced, the electrical resistance of this region is increased, thereby reducing transistor performance. Additionally, transistor performance is adversely affected by the reduction of SDE depth because current through the transistor needs to spread out from the thin accumulation layer.

Simply increasing the SDE depth, that is, its thickness, addresses the series resistance problem at the expense of having to tolerate short channel effects that are adverse to increased transistor performance. Conventional transistor structure engineering has focused on optimizing the trade-off between SDE depth and transistor performance, rather than trying to re-engineer the relationship between the thickness of the SDE and role of SDE thickness in inducing undesired short channel effects in MOSFETs.

Elevating the SDE region that is outside gate control, using , for example, a selective epitaxy process, can reduce the series resistance to a limited extent. However, because the SDE region under the gate, which is where most of the current spreading takes place, is not affected, the benefit of elevating the SDE region outside of gate control is of limited value. The elevated (also referred to as raised) SDE typically creates additional undesired gate-to-drain and gate-to-source overlap capacitance.

MOSFETs in accordance with an exemplary embodiment of the present invention include self-aligned, elevated SDE regions. More particularly, as can be seen in Figs. 2-4, the SDE regions are elevated with respect to the channel region. Because the elevated SDE regions underlie the gate electrode they are affected by the electric field induced by the charge on the gate electrode. This gate control effectively reduces the series resistance in the SDE regions. The SDEs in MOSFETs that embody the present invention can have increased thickness, relative to conventional MOSFETs, to reduce series resistance because the portion of the SDE that protrudes below the recessed central channel region is shallow, and therefore short channel effects are reduced. Furthermore, because the elevated SDE in accordance with the present invention is self-aligned to the gate electrode, overlap capacitance is reduced relative to conventional raised SDE structures.

Terminology

The terms, chip, integrated circuit, monolithic device, semiconductor device or component, and microelectronic device or component, and similar expressions are often used interchangeably in this field. The present invention is applicable to all the above as they are generally understood in the field.

The term "gate" is context sensitive and can be used in two ways when describing integrated circuits. As used herein, gate refers to the insulated gate terminal, also referred to as a gate electrode, of a three terminal FET when used in the context of transistor circuit configuration, and refers to a circuit for realizing

an arbitrary logical function when used in the context of a logic gate. A FET can be viewed as a four terminal device when the semiconductor body is considered.

Polycrystalline silicon is a nonporous form of silicon made up of randomly oriented crystallites or domains. Polycrystalline silicon is often formed by chemical vapor deposition from a silicon source gas or other methods and has a structure that contains large-angle grain boundaries, twin boundaries, or both. Polycrystalline silicon is often referred to in this field as polysilicon, or sometimes more simply as poly.

Source/drain terminals refer to the terminals of a FET, between which conduction occurs under the influence of an electric field, subsequent to the inversion of the semiconductor surface under the influence of an electric field resulting from a voltage applied to the gate terminal. Source/drain terminals are typically formed in a semiconductor substrate and have a conductivity type (i.e., p-type or n-type) that is the opposite of the conductivity type of the substrate. Sometimes, source/drain terminals are referred to as junctions. Generally, the source and drain terminals are fabricated such that they are geometrically symmetrical. Source/drain terminals may include extensions, sometimes referred to as tips, which are shallower than other portions of the source/drain terminals. The tips typically extend toward the channel region of a FET, from the main portion of the source/drain terminal. With geometrically symmetrical source and drain terminals it is common to simply refer to these terminals as source/drain terminals, and this nomenclature is used herein. Designers often designate a particular source/drain terminal to be a "source" or a "drain" on the basis of the voltage to be applied to that terminal when the FET is operated in a circuit.

Substrate, as used herein, refers to the physical object that is the basic workpiece that is transformed by various process operations into the desired microelectronic configuration. A substrate may also be referred to as a wafer. Wafers, may be made of semiconducting, non-semiconducting, or combinations of semiconducting and non-semiconducting materials.

The term vertical, as used herein, means substantially perpendicular to the surface of a substrate.

A schematic cross-section of a conventional FET is shown in Fig. 1. More particularly, as shown in Fig. 1, a substrate **102** has a gate dielectric layer **111** disposed over the surface thereof, and a patterned gate electrode is formed over gate dielectric layer **104** wherein the gate electrode has a polysilicon portion **108** and a silicided portion **107**. As shown, sidewall spacers **110** are disposed along laterally opposed sidewalls of the gate electrode. In this example of a conventional FET, substrate **102** is a silicon wafer, and gate dielectric layer **104** is a silicon dioxide layer.

Structural Examples

Figs. 2-4 show several illustrations of transistor structures which embody the present invention.

Fig. 2 shows a schematic cross-section of a MOSFET **200** illustrating one embodiment of the present invention. MOSFET **200** includes a gate dielectric **211** disposed over a portion of wafer **102**. It can be seen that, unlike the conventional MOSFET of Fig. 1, gate dielectric **211** conforms to a recess in wafer **102**. The recess has a bottom portions and substantially vertical sidewalls. A gate electrode is formed over gate dielectric **211**, the gate electrode having a polysilicon portion **208** and a silicide portion **107**. Sidewall spacers **110**, typically silicon nitride, are disposed adjacent the gate electrode. Source/drain extensions **205** are disposed adjacent gate dielectric **211**, and deep source/drain regions **204** are disposed substantially wafer **102** in a self-aligned fashion with respect to spacers **110**. The spatial relationship between deep source/drain regions **204**, source/drain extensions **205** and the channel region underlying gate dielectric **211**, are important in providing the electrical advantages of the present invention. By providing transistor **200** with a recessed channel region, source/drain extensions **205** may be elevated with respect thereto. In turn, by elevating source/drain extensions **205**, they may be made thicker for reduced

electrical resistivity, while appearing to be scaled down in thickness relative to their relationship with the channel region. Also, the innermost portions of source/drain extensions **205**, i.e., the portions nearest to the channel region, have a portion of the gate electrode overlying them. This arrangement is also believed to provide improvements in electrical performance.

Fig. 3 shows a schematic cross-section of a MOSFET **300** illustrating an alternative embodiment of the present invention. MOSFET **300** includes a gate dielectric **311** disposed over a portion of wafer **102**. It can be seen that, unlike the conventional MOSFET of Fig. 1, gate dielectric **311** conforms to a recess in wafer **102**. The recess has a bottom portions and tapered sidewalls. Typically, these tapered sidewalls form an angle greater than 90° with respect to the bottom portion of the recess. A gate electrode is formed over gate dielectric **311**, the gate electrode having a polysilicon portion **308** and a silicide portion **107**. Sidewall spacers **110**, typically silicon nitride, are disposed adjacent the gate electrode. Source/drain extensions **305** are disposed adjacent gate dielectric **311**, and deep source/drain regions **304** are disposed substantially wafer **102** in a self-aligned fashion with respect to spacers **110**. The spatial relationship between deep source/drain regions **304**, source/drain extensions **305** and the channel region underlying gate dielectric **311**, are important in providing the electrical advantages of the present invention. By providing transistor **300** with a recessed channel region, source/drain extensions **305** may be elevated with respect thereto. In turn, by elevating source/drain extensions **305**, they may be made thicker for reduced electrical resistivity, while appearing to be scaled down in thickness relative to their relationship with the channel region.

Fig. 4 shows a schematic cross-section of a MOSFET **400** illustrating another alternative embodiment of the present invention. MOSFET **400** includes a gate dielectric **411** disposed over a portion of wafer **102**. It can be seen that, unlike the conventional MOSFET of Fig. 1, gate dielectric **411** conforms to a recess in the wafer **102**. The recess has a curvilinear surface. A gate electrode is formed over gate dielectric **411**, the gate electrode having a polysilicon portion

408 and a silicide portion **107**. Sidewall spacers **110**, typically silicon nitride, are disposed adjacent the gate electrode. Source/drain extensions **405** are disposed adjacent gate dielectric **411**, and deep source/drain regions **404** are disposed substantially wafer **102** in a self-aligned fashion with respect to spacers **110**. The spatial relationship between deep source/drain regions **404**, source/drain extensions **405** and the channel region underlying gate dielectric **411**, are important in providing the electrical advantages of the present invention. By providing transistor **400** with a recessed channel region, source/drain extensions **405** may be elevated with respect thereto. In turn, by elevating source/drain extensions **405**, they may be made thicker for reduced electrical resistivity, while appearing to be scaled down in thickness relative to their relationship with the channel region.

Many variations are possible within the scope of the present invention. For example, gate dielectric layer **104** is typically a thin layer of oxidized silicon, but the thickness and chemical make-up of gate dielectric layer **104** may be varied within the scope of the invention. Similarly, it will be clear to those skilled in the art, that silicide layers **106**, **107** may be formed from various metals, including but not limited to, titanium, tungsten, nickel, cobalt, and molybdenum; and silicide layers **106**, **107** are not required to be of the same material or the same thickness. In further alternatives, transistors in accordance with the present invention may be formed without silicide layers, and may further be formed with metal gate electrodes rather than polysilicon gate electrodes. Sidewall spacers **110** are typically formed of silicon nitride, but other suitable materials may be substituted, and the sidewall spacers may be comprised of more than one layer of material. In still further alternatives, the transistor may be formed with silicon germanium source/drain terminals. The foregoing description of alternative materials and structures is for illustrative purposes only, and is not intended as an exhaustive list of alternatives. Those skilled in the art will undoubtedly recognize further variations within the scope of the invention.

Process Examples

Processes embodying the present invention include a damascene transistor flow coupled with a self-aligned channel recess etch. No special equipment, other than that typically used for producing MOS integrated circuits is required. In typical embodiments, channel implant operations are performed on a silicon wafer in a conventional manner, an etch stop layer, typically silicon dioxide, and a damascene layer, typically silicon nitride, are then formed over the wafer. The damascene layer is then patterned using a reverse tone polysilicon (i.e., gate electrode) mask. Alternatively the damascene layer is patterned using the conventional polysilicon mask with a negative photoresist. The patterning of the damascene layer results in openings being formed in areas where the gate electrodes are to be formed. Typically, the etch stop layer at the bottom of the damascene layer opening is removed, and a first spacer may then be formed along the sidewalls of the openings in the damascene layer. These first spacers define regions of the channel that will be recessed. Several alternative processes for recessing the channel are available. For example, in one embodiment an anisotropic etch (e.g., dry etch) of the exposed silicon is performed to recess the transistor channel region. In another embodiment, the exposed silicon is first oxidized, and the oxide is then etched, resulting in a recess with a tapered, rather than vertically abrupt, transition edge. In a further alternative embodiment, the channel recess etch is performed using an isotropic etch (e.g., wet etch) of the exposed silicon, which results in a curvilinear shape for the channel recess. IN relation to the recessed channel, the source/drain extension are elevated.

After the channel recess operation, a gate dielectric, typically an oxide of silicon, is formed over the surface of the channel recess. A material, such as, but not limited to, polysilicon, may then be deposited over the surface of the wafer. A planarization operation, typically chemical mechanical polishing using the damascene layer as an etch stop, is then performed. The damascene and underlying etch stop layers are then removed and source/drain extensions are

formed, typically by ion implantation. Spacers are then formed along laterally opposed sidewalls of the gate electrodes. These spacers are often referred to as sidewall spacers. Deep source/drain regions are then formed, aligned to the sidewall spacers, typically by ion implantation.

Further description of illustrative processes embodying the present invention are provided below in connection with Figs. 5-22.

A first process embodying the present invention is described in conjunction with Figs. 5-12. Referring to Fig. 5, a silicon wafer **102** has an etch stop layer **502** formed thereon. Etch stop layer **502** is typically, but not required to be an oxide of silicon. Etch stop layer **502** may be formed by thermal oxidation of the surface of wafer **102**, or by well-known deposition processes. A layer **504**, referred to hereinafter as a damascene layer, is formed over etch stop layer **502**. Damascene layer **504** is typically a deposited layer of silicon nitride.

After deposition, damascene layer **504** is patterned, so as to form openings therein. Patterning is typically performed with well-known photolithography processes. The openings in damascene layer **504** have substantially vertical sidewalls, but this is not a requirement of the present invention. These openings correspond to the locations of transistor gate electrodes which are to be formed in a later stage of the process. The openings in damascene layer **504** expose portions of underlying etch stop layer **502**. The exposed portions of etch stop layer **502** is removed to expose the underlying silicon wafer **102**. Fig. 6 shows the structure of Fig. 5 after the patterning of layers **504** and **502**.

Referring to Fig. 7, the structure of Fig. 6 is shown after two sets of spacers have been formed adjacent the vertical sidewalls of the openings in layers **504**, **502**. A first spacer **508** is formed immediately adjacent to the sidewalls of the openings and a second spacer **510** is formed adjacent first spacer **508**, as shown in Fig. 7. First spacer **508** is typically formed from silicon nitride which has been deposited by CVD and then subjected to an anisotropic

etch. Second spacer **510** is typically formed from silicon dioxide which has been deposited by CVD and then subjected to an anisotropic etch.

Fig. 8 shows the structure of Fig. 7 after a recess **512** is formed in wafer **102**. The recess in the wafer **102** is formed by an anisotropic etch process (e.g., dry etching of silicon). Recess **512** has a bottom portion **514** and substantially vertical sidewalls **516**.

Subsequent to formation of recess **512**, second spacer **510** is removed, the exposed silicon surface is oxidized to form a gate dielectric layer **511**, and polysilicon **518** is deposited over the surface of wafer **102** as shown in Fig. 9. Those skilled in the art and having the benefit of this disclosure will recognize, that gate dielectric layer **511** may be formed in other ways or with other materials. The thickness and chemical composition of the gate dielectric may vary widely within the scope of the present invention.

Wafer **102** with polysilicon **518** over the surface thereof is planarized, typically by chemical mechanical polishing (CMP). The CMP operation uses damascene layer **504** as a polish stop. The results of the CMP operation, shown in Fig. 10, illustrate newly formed gate electrode **520**.

Fig. 11 shows the structure of Fig. 10 after the removal of damascene layer **504**, etch stop layer **502**, and first spacer **508**. More particularly, Fig. 11 shows polysilicon gate electrode **520** disposed superjacent gate dielectric **511**, which is formed over the surface of the recessed channel as shown in the figure.

Fig. 12 shows the structure of Fig. 11, after conventional semiconductor processing operations are used to implant source/drain extensions **524**, self-aligned to gate electrode **520**, form sidewall spacers **110**, implant deep source/drains **522**, and form silicide regions **106** and **107**.

An alternative embodiment is described in conjunction with Figs. 5-7 and 13-17. In this alternative illustrative embodiment, the processing operations as described above in connection with Figs. 5-7 are performed as before. However, referring to Fig. 13, rather than anisotropically etching the exposed silicon

surface, the exposed silicon surface is first oxidized, and then the oxidized silicon is removed, resulting in a recess **612** having a bottom portion **614** and tapered sidewalls **616**.

Fig. 14 shows the structure of Fig. 13, after the further processing operations of forming a gate dielectric layer **611** over a bottom portion **614** and tapered sidewalls **616** of recess **612**. Gate dielectric **611** is typically formed by oxidizing the exposed silicon surfaces of recess **612**. Those skilled in the art and having the benefit of this disclosure will recognize, that gate dielectric layer **611** may be formed in other ways or with other materials. The thickness and chemical composition of the gate dielectric may vary widely within the scope of the present invention.

Fig. 15 shows the structure of Fig. 14, after the further processing operations of forming individual gate electrodes **620** by removing the excess polysilicon. Gate electrode **620** is formed from polysilicon **618** by a CMP operation with damascene layer **504** acting as the polish stop layer. CMP of polysilicon is a well-known process operation in this field. Fig. 16 shows the structure of Fig. 15, after damascene layer **504**, etch stop layer **502**, and first spacer layer **508** are removed by etching. As can be seen, polysilicon gate electrode **620** is disposed superjacent gate dielectric **611**, which is formed over the surface of the recessed channel as shown in the figure.

Fig. 17 shows the structure of Fig. 16, after conventional semiconductor processing operations are used to implant source/drain extensions **624**, self-aligned to gate electrode **620**, form sidewall spacers **110**, implant deep source/drains **622**, and form silicide regions **106** and **107**.

A further alternative embodiment is described in conjunction with Figs. 5-7 and 18-22. In this alternative illustrative embodiment, the processing operations as described above in connection with Figs. 5-7 are performed as before. However, referring to Fig. 18, in this embodiment the exposed silicon surface is isotropically etched, resulting in a recess **712** having a curvilinear surface **714**.

Fig. 19 shows the structure of Fig. 18, after the further processing operations of forming a gate dielectric layer **711** over curvilinear surface **714** of recess **712**, the removal of second spacer **510** and the deposition of polysilicon layer **718**. Gate dielectric **711** is typically formed by oxidizing the exposed silicon surface of recess **712**. Those skilled in the art and having the benefit of this disclosure will recognize, that gate dielectric layer **711** may be formed in other ways or with other materials. The thickness and chemical composition of the gate dielectric may vary widely within the scope of the present invention.

Fig. 20 shows the structure of Fig. 19, after the further processing operations of forming individual gate electrodes **720** by removing the excess polysilicon. Gate electrode **720** is formed from polysilicon **718** by a CMP operation with damascene layer **504** acting as the polish stop layer. CMP of polysilicon is a well-known process operation in this field. Fig. 21 shows the structure of Fig. 20, after damascene layer **504**, etch stop layer **502**, and first spacer layer **508** are removed by etching. As can be seen, polysilicon gate electrode **720** is disposed superjacent gate dielectric **711**, which is formed over the surface of the recessed channel as shown in the figure.

Fig. 22 shows the structure of Fig. 21, after conventional semiconductor processing operations are used to implant source/drain extensions **705**, self-aligned to gate electrode **720**, form sidewall spacers **110**, implant deep source/drains **704**, and form silicide regions **106** and **107**.

In a further alternative, channel implants, typically performed prior to the formation of damascene layer **504**, are performed after damascene layer **504**, and etch stop layer **502** are patterned, and first and second spacers **508**, **510** are formed along the sidewalls of the openings in damascene layer **504**. As will be understood by those skilled in this field, by having the channel implant self-aligned to the transistor gate, junction capacitance is reduced, and, depending on the actual doping profiles of the channel implant, source/drain extension implant, and deep source/drain implant, counterdoping effects may also be reduced.

Fig. 23 is a flow diagram illustrating a process flow in accordance with the present invention. Openings are patterned, typically with conventional lithography techniques, in a damascene layer disposed on a wafer (block **2302**). Spacers are then formed along the sidewalls of the openings in the damascene layer (block **2304**). Typically a first spacer layer, such as an oxide of silicon, is formed and a second spacer layer, typically a nitride of silicon, is formed adjacent to the first spacer layer. A recess is then formed at the locations defined by the openings (block **2306**). The specific shape of the recesses may be varied within the scope of the present invention. For example, recesses may be shaped rectangularly, trapezoidally, curvilinearly, and so on. The various shapes may be achieved by applying corresponding various etch techniques. Isotropic and anisotropic etching are two examples. A gate dielectric is then formed over the recess (block **2308**) and a gate electrode is formed over the gate dielectric (block **2310**). Source/drain extensions are formed, typically by ion implantation, self-aligned to the gate electrode (block **2312**).

Conclusion

Embodiments of the present invention advantageously provide a field effect transistor structure having very short channel length and relatively low source/drain extension resistivity without the adverse short channel effects of conventional MOSFETs having equivalent channel lengths and source/drain extension resistivities. Embodiments of the present invention have source/drain extensions that are elevated relative the channel region of a MOSFET

A further advantage of particular embodiments of the present invention is reduced parasitic junction capacitance resulting from performing the channel implant only into portions of the wafer that will become the channel regions of transistors.

Those skilled in the art and having the benefit of this disclosure will recognize that although field oxide regions are not shown in the Figures, the operations and structures shown and described herein, are compatible with

various field oxide isolation architectures. Examples of field oxide isolation architectures include shallow trench isolation regions in a surface of a substrate, and the older local oxidation of silicon, which often formed non-planarized oxide isolation regions.

It will be understood by those skilled in the art having the benefit of this disclosure that many design choices are possible within the scope of the present invention. For example, structural parameters, including but not limited to, gate insulator thickness, gate insulator materials, gate electrode thickness, sidewall spacer material, inter-layer dielectric material, isolation trench depth, and S/D and well doping concentrations may all be varied from that shown or described in connection with the illustrative embodiments.

It will be understood that various other changes in the details, materials, and arrangements of the parts and steps which have been described and illustrated may be made by those skilled in the art having the benefit of this disclosure without departing from the principles and scope of the invention as expressed in the subjoined Claims.

What is claimed is:

1. A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having a bottom portion and substantially vertical sidewalls;

a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the substantially vertical sidewalls;

a gate electrode overlying the gate dielectric layer; and

source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;

wherein the source/drain terminals have an extension which extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess.

2. The transistor of Claim 1, further comprising a portion of the gate electrode that overlies an innermost portion of the source/drain extension:

3. The structure of Claim 2, wherein the gate electrode conforms to the recessed channel.

4. A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having bottom portion and tapered sidewalls, the tapered sidewall surfaces forming an obtuse angle with respect to the bottom portions of the recess;

a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the tapered sidewalls;

a gate electrode overlying the gate dielectric layer; and

source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;

wherein the source/drain terminals have an extension which extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess.

5. The transistor of Claim 4, wherein a portion of the gate electrode that overlies an innermost portion of the source/drain extension.

6. The transistor of Claim 4, wherein the gate electrode conforms to the recessed channel.

7. A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having a curvilinear shape;

a gate dielectric layer disposed superjacent the curvilinear recess;

a gate electrode overlying the gate dielectric layer; and

source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;

wherein the source/drain terminals have an extension which extends downwardly, from approximately the surface of the substrate, along the curvilinear sides of the recess.

8. The transistor of Claim 6, wherein a portion of the gate electrode that overlies an innermost portion of the source/drain extension.

9. The transistor of Claim 6, wherein the gate electrode conforms to the recessed channel.

10. A method of making a microelectronic device, comprising:

forming a first layer over a substrate;

forming openings in the first layer, the openings exposing a portion of the substrate, the openings having substantially vertical sidewalls;

forming a first spacer adjacent the sidewalls of the first layer openings;

forming a second spacer adjacent the first spacer;

etching a portion of the exposed substrate;

removing the second spacer;

forming a dielectric layer superjacent the exposed portions of the substrate;

forming an electrode superjacent the dielectric layer; and

removing the first layer.

11. The method of Claim 10, wherein etching a portion of the exposed substrate comprises isotropically etching the substrate.

12. The method of Claim 10, wherein etching a portion of the exposed substrate comprises anisotropically etching the substrate.

13. The method of Claim 10, further comprising oxidizing the exposed portions of the substrate, and wherein the etching a portion of the exposed substrate comprises etching the oxidized portions of the substrate.

14. A method of forming a field effect transistor, comprising:

depositing an etch stop layer and a damascene layer over a silicon substrate;

removing portions of the damascene and etch stop layers to expose portions of the silicon, and form sidewalls in the damascene and etch stop layers;

forming a first spacer layer along the sidewalls of the damascene layer and the etch stop layer;

etching the exposed silicon;

removing the second spacer; forming a gate dielectric layer superjacent the etched silicon; and depositing a gate electrode layer over the damascene and gate dielectric layers;

planarizing the gate electrode layer so as to form a gate electrode;

removing the damascene, second spacer, and etch stop layers; and

forming source/drain terminals self-aligned to the gate electrode.

15. The method of Claim 14, wherein planarizing the gate electrode layer comprises chemical mechanical polishing using the damascene layer as a polish stop.

16. The method of Claim 14, further comprising implanting ions into the silicon substrate.

17. The method of Claim 14, further comprising implanting ions into the silicon substrate, after the first and second spacers are formed.

18. The method of Claim 14, further comprising performing a channel implant into the silicon using the damascene, first spacer, and second spacer layers as implant masks.

19. The method of Claim 14 wherein forming source/drain terminals comprises implanting ions of a first conductivity type into the silicon, adjacent to the gate electrode; forming third spacers adjacent to the gate electrode, and implanting ions of a first conductivity type into the silicon, adjacent to the third spacers.

20. The method of Claim 14, wherein etching the silicon comprises an anisotropic etch.

21. The method of Claim 14, wherein etching the silicon comprises an isotropic etch.

22. A method of forming a field effect transistor, comprising:

depositing an etch stop layer and a damascene layer over a silicon substrate;

removing portions of the damascene and etch stop layers to expose portions of the silicon, and form sidewalls in the damascene and etch stop layers;

forming a first spacer layer along the sidewalls of the damascene layer and the etch stop layer, and a second spacer adjacent the first spacer layer;

oxidizing the exposed silicon;

etching the exposed oxidized silicon;

removing the second spacer; forming a gate dielectric layer superjacent the etched silicon; and depositing a gate electrode layer over the damascene and gate dielectric layers;

planarizing the gate electrode layer so as to form a gate electrode;

removing the damascene, second spacer, and etch stop layers; and

forming source/drain terminals self-aligned to the gate electrode.

ABSTRACT OF THE DISCLOSURE

Field effect transistor structures include a channel region formed in a recessed portion of a substrate. The recessed channel portion permits the use of relatively thicker source/drain regions thereby providing lower source/drain extension resistivity while maintaining the physical separation needed to overcome various short channel effects. The surface of the recessed channel portion may be of a rectangular, polygonal, or curvilinear shape. In a further aspect of the present invention, transistors are manufactured by a process in which a damascene layer is patterned, the channel region is recessed by etch that is self-aligned to the patterned damascene layer, and the gate electrode is formed by depositing a material over the channel region and patterned damascene layer, polishing off the excess gate electrode material and removing the damascene layer.

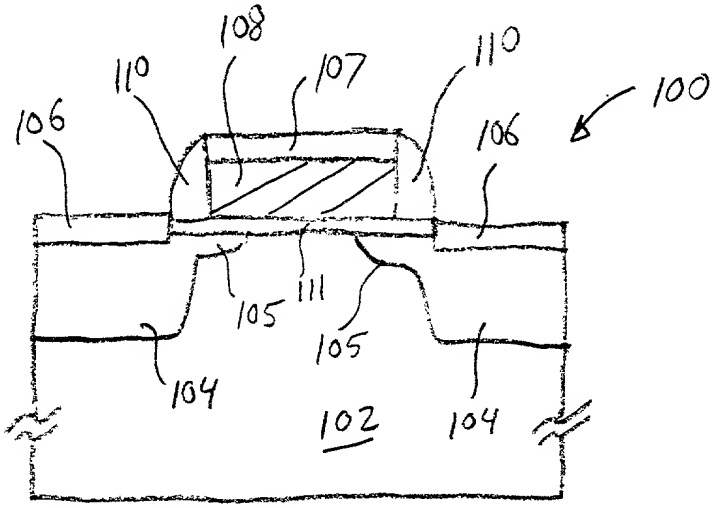

Fig. 1

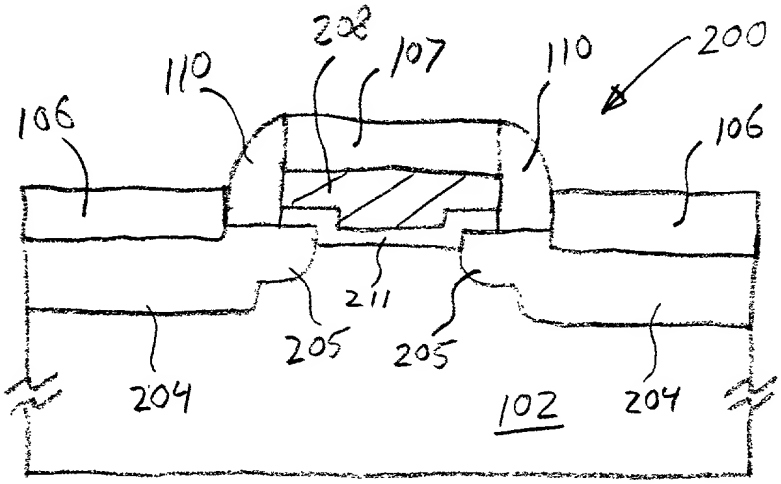

Fig. 2

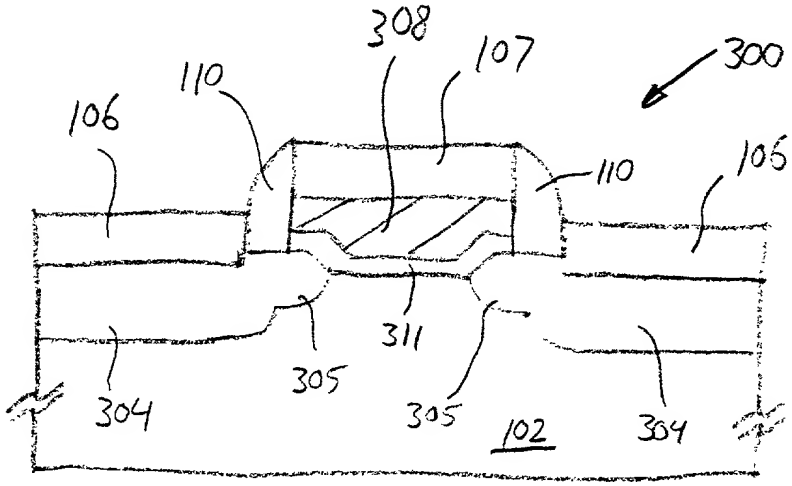

Fig. 3

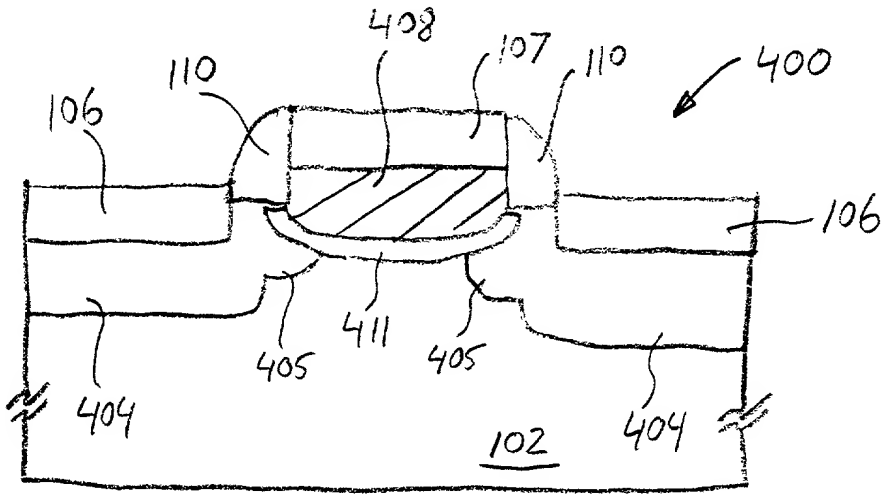

Fig. 4

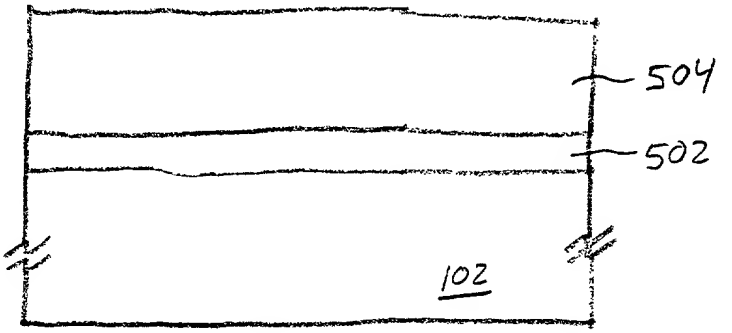

Fig. 5

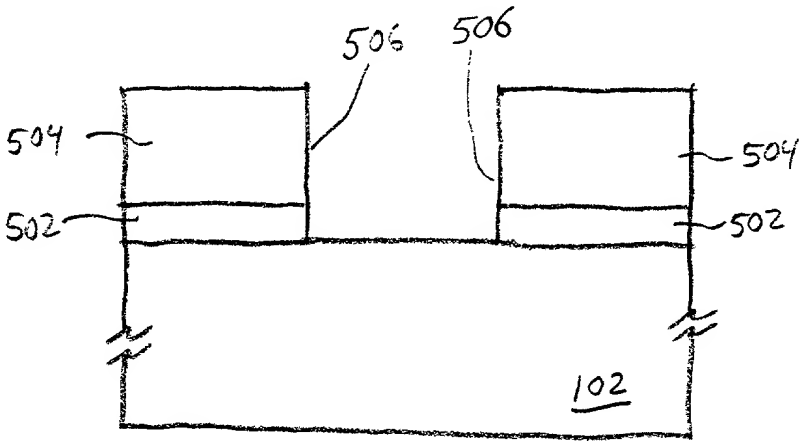

Fig. 6

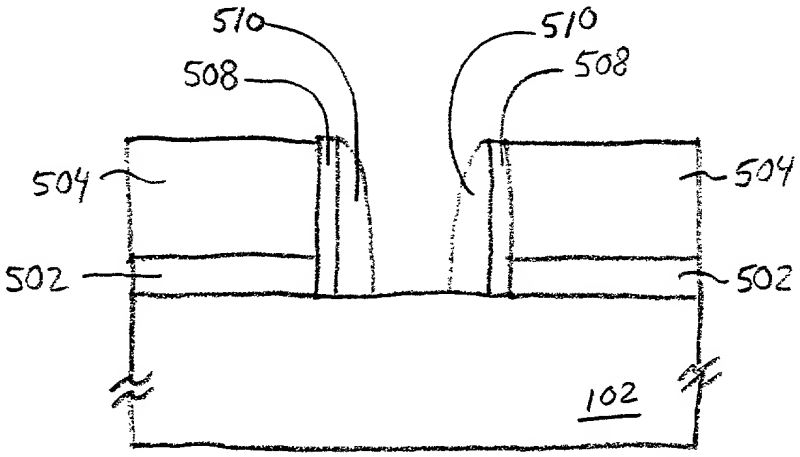

Fig. 7

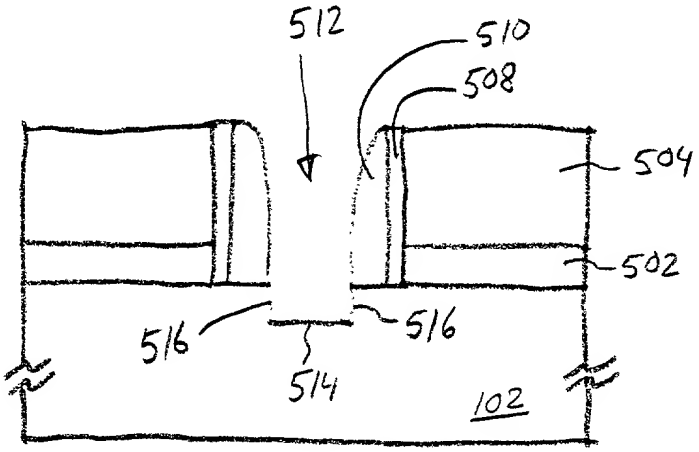

Fig. 8

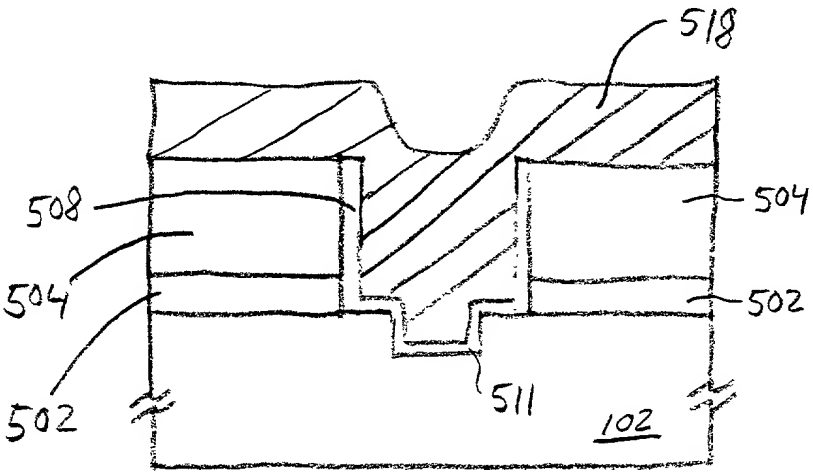

Fig. 9

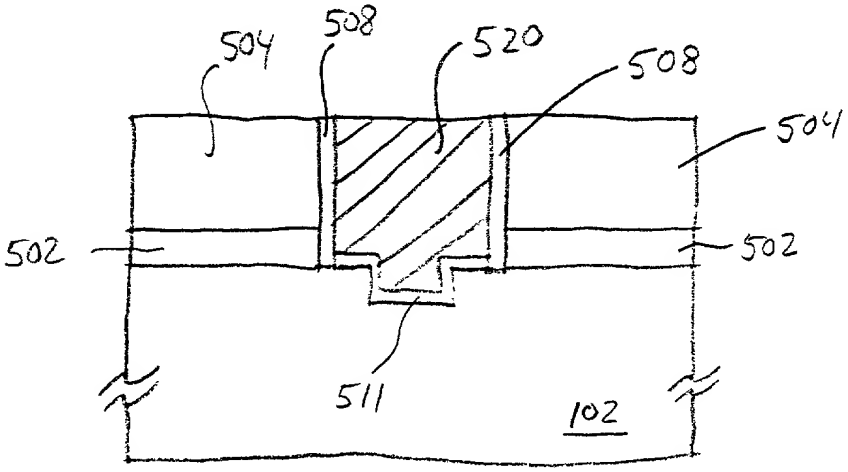

Fig. 10

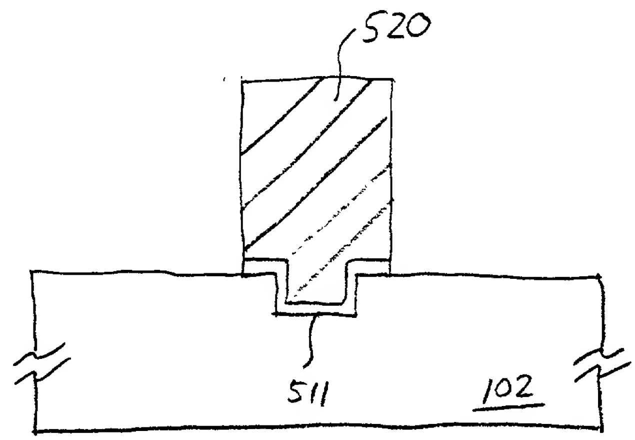

Fig. 11

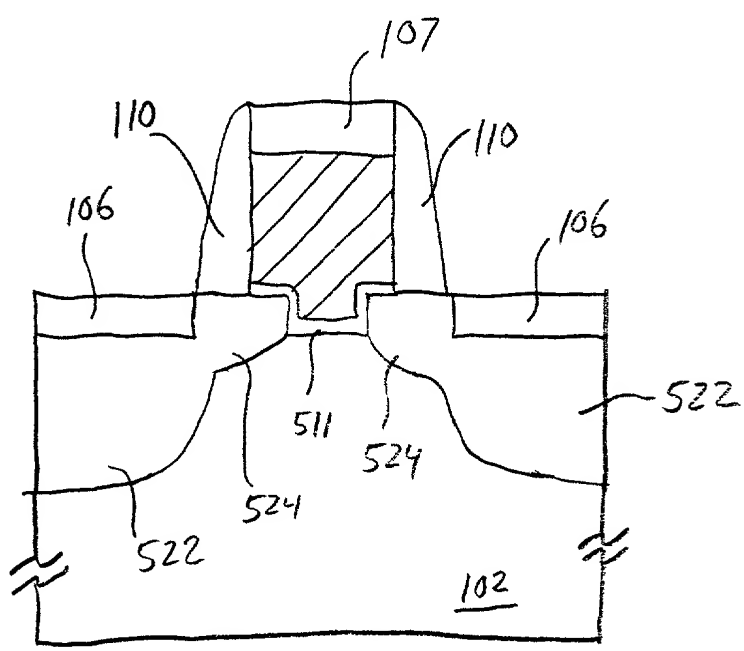

Fig. 12

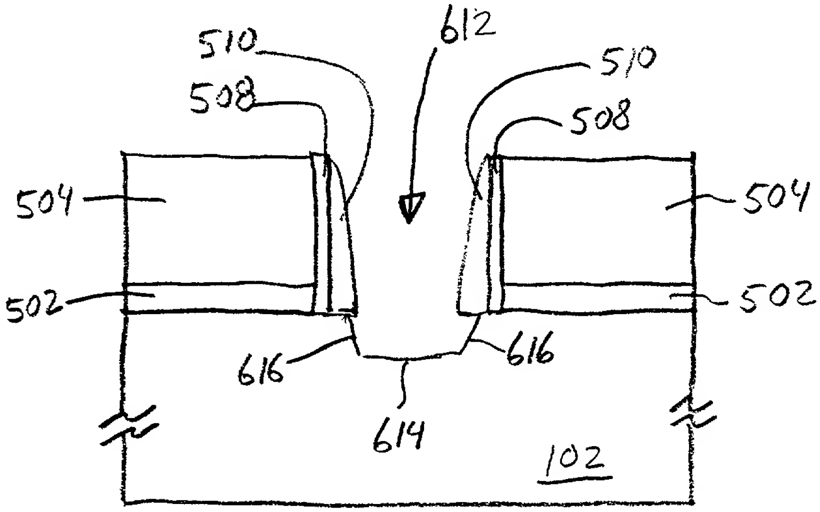
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Fig. 13

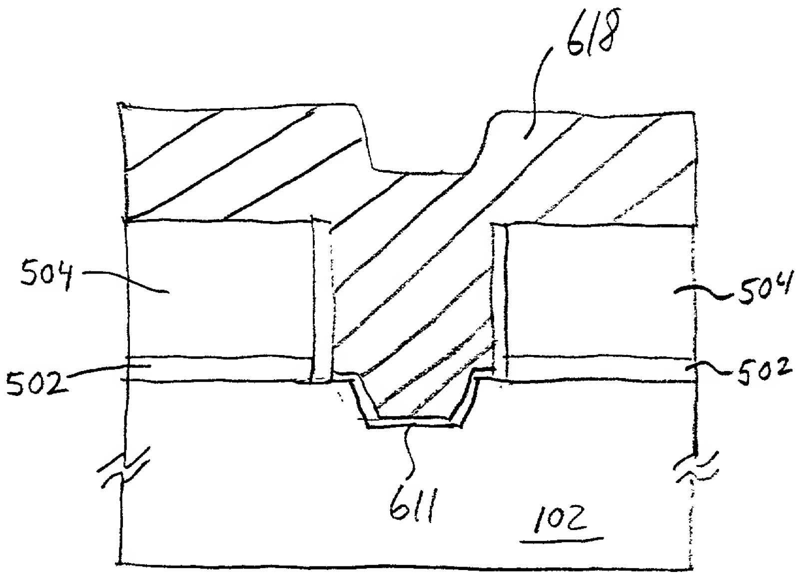
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Fig. 14

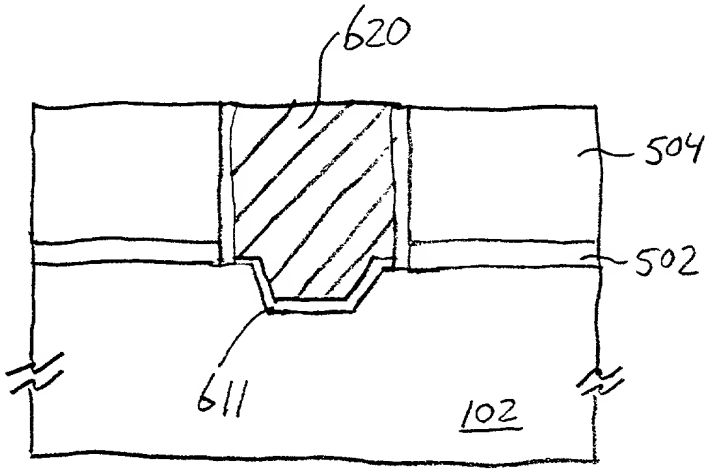

Fig. 15

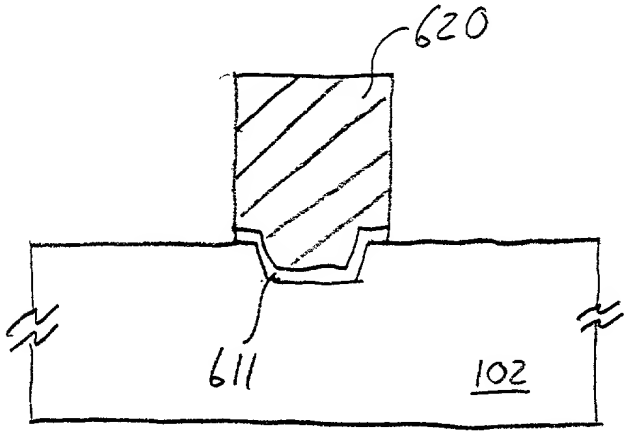

Fig. 16

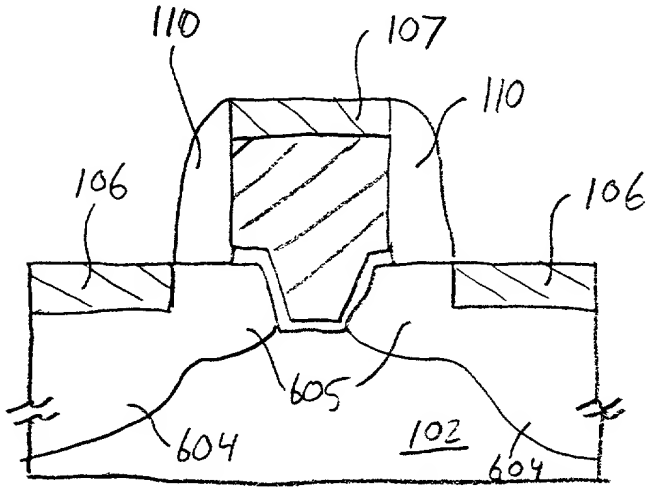

Fig. 17

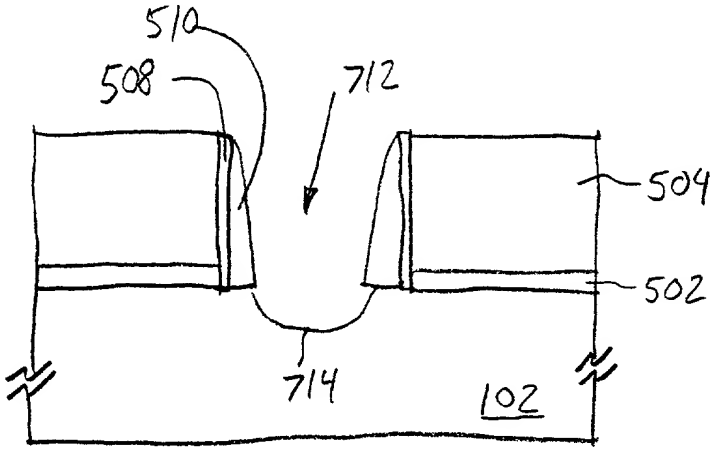

Fig. 18

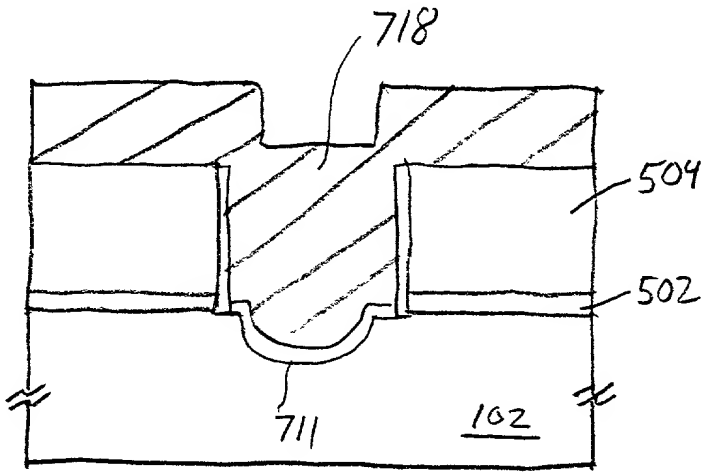

Fig. 19

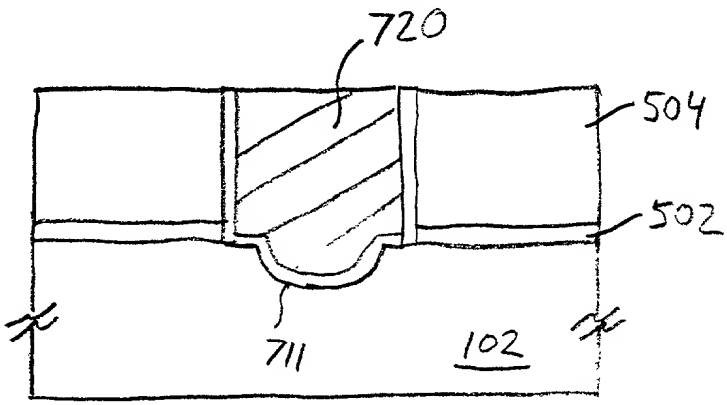

Fig. 20

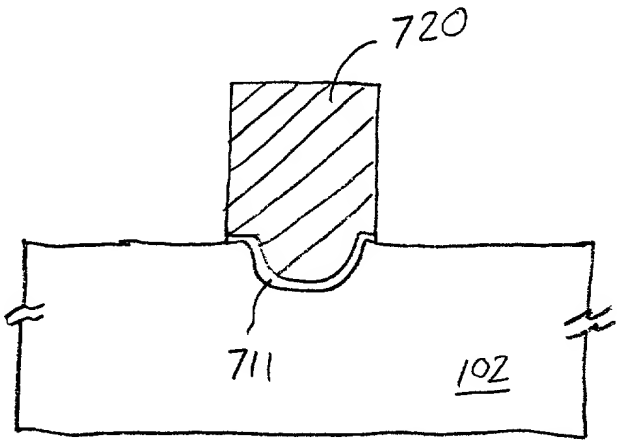

Fig. 21

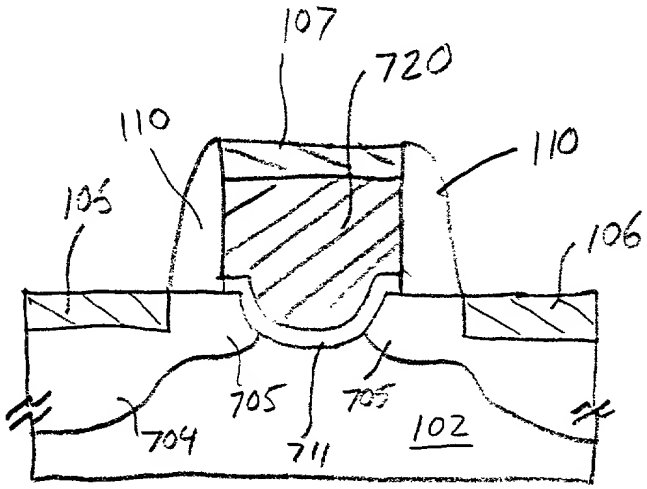

Fig. 22

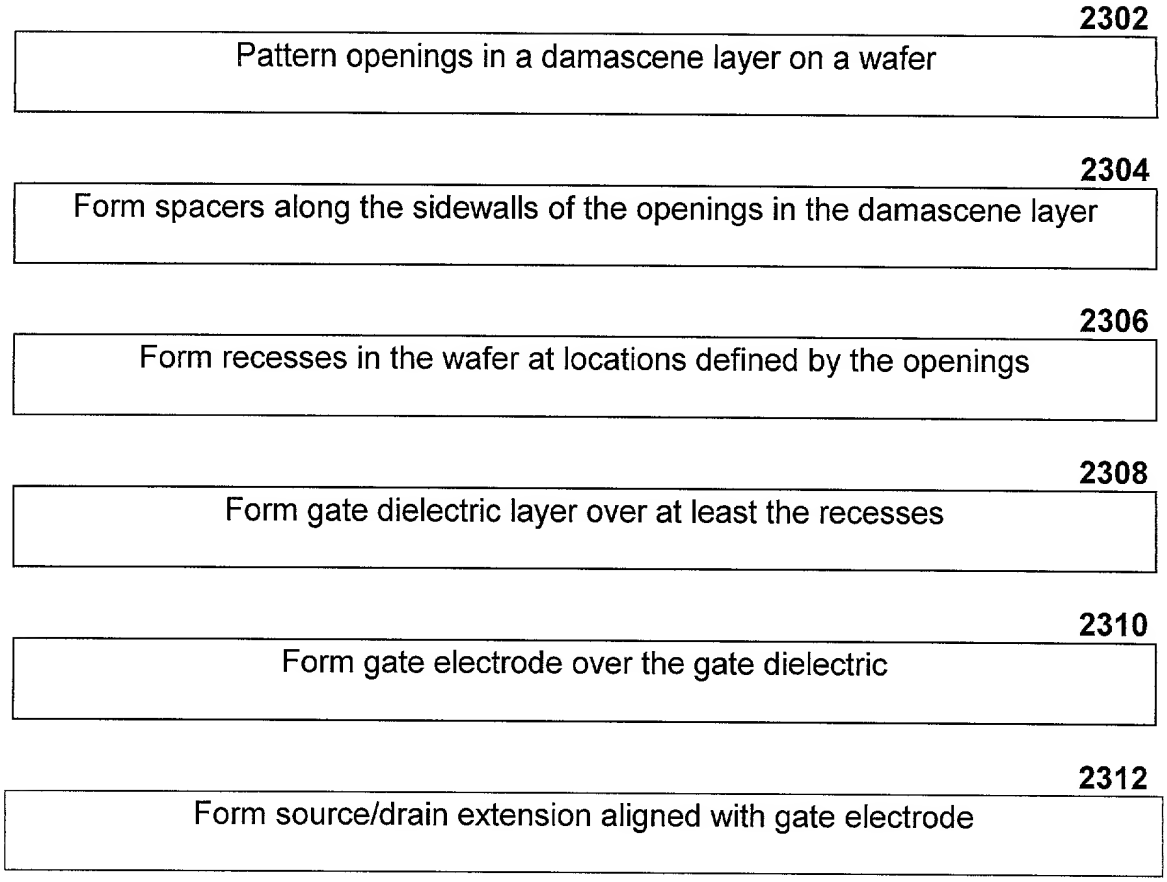
2302
Pattern openings in a damascene layer on a wafer
2304
Form spacers along the sidewalls of the openings in the damascene layer
2306
Form recesses in the wafer at locations defined by the openings
2308
Form gate dielectric layer over at least the recesses
2310
Form gate electrode over the gate dielectric
2312
Form source/drain extension aligned with gate electrode

FIG. 23

Attorney's Docket No.: 042390.P6892

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

FIELD EFFECT TRANSISTOR STRUCTURE WITH SELF-ALIGNED RAISED SOURCE/DRAIN EXTENSIONS

the specification of which

[X] is attached hereto.
[ ] was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____ .
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, **month**, year)	PRIORITY CLAIMED UNDER 37 USC 119
			☐ No ☐ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, a firm including: William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432: William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Ronald C. Card, Reg. No. 44,587; Thomas M. Coester, Reg. No. 39,637; Donna Jo Coningsby, Reg. No. 41,684; Stephen M. De Klerk, under 37 C.F.R. § 10.9(b); Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Matthew C. Fagan, Reg. No. 37,542; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. P41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Erica W. Kuo, Reg. No. 42,775; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. 42,004; Lisa A. Norris, Reg. No. P44,976; Chun M. Ng, Reg. No. 36,878; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Dennis A. Nicholls, Reg. No. 42,036; Kimberley G. Nobles, Reg. No. 38,255; Daniel E. Ovanezian, Reg. No. 41,236; Babak Redjaian, Reg. No. 42,096; William F. Ryann, Reg. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey Sam Smith, Reg. No. 39,377; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; John F. Travis, Reg. No. 43,203; George G. C. Tseng, Reg. No. 41,355; Joseph A. Twarowski, Reg. No. 42,191; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John Patrick Ward, Reg. No. 40,216; Charles T. J. Weigell, Reg. No. 43,398; Kirk D. Williams, Reg. No. 42,229; James M. Wu, Reg. No. P45,241; Steven D. Yates, Reg. No. 42,242; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and Andrew C. Chen, Reg. No. 43,544; Justin M. Dillon, Reg. No. 42,486; Paramita Ghosh, Reg. No. 42,806; and Sang Hui Kim, Reg. No. 40,450; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Jeffrey S. Draeger, Reg. No. 41,000; Cynthia Thomas Faatz, Reg No. 39,973; Sean Fitzgerald, Reg. No. 32,027; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Charles A. Mirho, Reg. No. 41,199; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Kenneth M. Seddon, Reg. No. 43,105; Mark Seeley, Reg. No. 32,299; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; Robert G. Winkle, Reg. No. 37,474; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells; Reg. No. P43,256, Peter Lam, Reg. No. P44,855; and Gene I. Su, Reg. No. 45,140; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Raymond J. Werner, Reg. No. 34,752, BLAKELY, SOKOLOFF, TAYLOR &
(Name of Attorney or Agent)
ZAFMAN LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to Raymond J. Werner, Reg. No. 34,752, (503) 684-6200.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor (given name, family name) **Kaizad R. Mistry**

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City , State) *(Country)*

P. O. Address _____

_____

Full Name of Second/Joint Inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City , State) *(Country)*

P. O. Address _____

_____

Full Name of Third/Joint Inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City , State) *(Country)*

P. O. Address _____

_____

Full Name of Fourth/Joint Inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City , State) *(Country)*

P. O. Address _____

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